Returning to FIG. **27**, after forming the annular gate dielectric layer **206** and the annular gate **207**, a lightly doped region may be formed (S**104**). FIG. **8** illustrates a corresponding semiconductor structure; and FIG. **9** illustrates a cross-section view of the semiconductor structure illustrated in FIG. **8** along the A-A direction.

As shown in FIG. **9**, an annular lightly doped region **210** is formed in the well region **202** at the outer side of the annular gate **207**. The annular lightly doped region **210** may reduce the breakdown point of an avalanche effect of an LDMOS transistor, thus the breakdown voltage may be reduced.

In one embodiment, the annular lightly doped region **210** may be formed by forming a hard mask layer (not shown) exposing a portion of the well region **202** at the outer side of the annular gate **207** on the annular gate **207** and the semiconductor substrate **201**; and forming the annular lightly doped region **210** by an ion implantation process onto the portion of the well region **202** at the outer side of the annular gate **207**. When the semiconductor substrate **201** is used to form N-type LDMOS transistors, the annular lightly doped region **210** may be doped with N-type ions. When the semiconductor substrate **201** is used to form P-type LDMOS transistors, the annular lightly doped region **210** may be doped with P-type ions.

In certain other embodiments, the annular lightly doped region **210** may be omitted.

Referring to FIG. **9**, after forming the annular lightly doped region **210**, sidewall spacers **208** may be formed on the side surfaces of the annular gate **207** and the annular gate dielectric layer **206**. The sidewall spacers **208** at the outer side of the annular gate **207** and the annular gate dielectric layer **206** and the annular lightly doped region **210** may have an annular overlap along a direction vertical to the surface of the semiconductor substrate **201**.

Various processes may be used to form the sidewall spacers **208**, in one embodiment, the sidewall spacers **208** may be formed by forming a sidewall spacer material layer on the semiconductor substrate **201** and the annular gate **207**, and around the annular gate **207** and the annular gate dielectric layer **206**; and performing an etch back process to remove the sidewall spacer material layer on the semiconductor substrate **201** and the annular gate **207**. Thus, the sidewall spacers **208** on the side surfaces of the annular gate **207** and the annular gate dielectric layer **206** may be formed.

The sidewall spacer material layer may be made of any appropriate material, such as silicon oxide, silicon nitride, or silicon oxynitride, etc. The sidewall spacers **208** may also be stacked layers made of different materials. Various processes may be used to form the sidewall spacer material layer, such as a CVD process, a PVD process, or an ALD process, etc. The etch back process may be a dry etching process, or a wet chemical etching process, etc.

Returning to FIG. **27**, after forming the sidewall spacers **208**, a source region and a drain region may be formed (S**105**). FIG. **8** illustrates a corresponding semiconductor structure; and FIG. **9** illustrates a cross-section view of the semiconductor structure illustrated in FIG. **8** along the A-A direction.

As shown in FIG. **8** and FIG. **9**, an annular source region **209** is formed in the annular lightly doped region **210**, and a drain region **205** is formed in drifting region **203** at the inner side of the isolation structure **204**. Referring to FIG. **9**, a depth of the source region **209** may be smaller than a depth of the annular lightly doped region **210**. The annular source region **209** and the drain region **205** may be formed by any appropriate process, such as an ion implantation process, or an embedding method, etc.

Thus, the LDMOS transistor may include an annular gate **207**, a drain region **205** in drafting region **203** at the inner side of the annular gate **207**, and an annular source region **209** in the lightly doped region **210** at outer side of the annular gate **207**. An annular channel may be formed between the drain region **205** and the annular source region **209**. The annular gate **207** may control the annular channel from different directions, thus the LDMOS transistor may have an enhanced channel control ability. Therefore, a short-channel effect may be effectively reduced, and the drive current may be increased. Further, the LDMOS transistor may occupy less area of a chip under a same drive current, thus the production cost may be reduced.

Thus, a LDMOS transistor may be formed by the above disclosed processes and methods, the corresponding transistor is illustrated in FIG. **8**; and FIG. **9** illustrates a cross-section view of the LDMOS transistor shown in FIG. **8**. The LDMOS transistor includes a semiconductor substrate **201** having a well region **202** and a drifting region **203** in the well region **202**. The LDMOS transistor also includes a drain region **205** in the drifting region **203** and an annular isolation structure **204** surrounding the drain region **205**. Further, the LDMOS transistor includes an annular gate dielectric layer **206** on the well region **202** and an annular gate **207** on an annular gate dielectric layer **206**. Further, the LDMOS transistor also includes sidewall spacers **208** around the annular gate dielectric layer **206** and the annular gate **207**, and an annular source region **209** in a lightly doped region **210** at the outer side of the sidewall spacers **208**. The detailed structures and intermediate structures are described above with respect to the fabrication methods.

FIGS. **10**, **12**, **14** and **16** illustrate semiconductor structures corresponding to certain stages of the exemplary fabrication process of another LDMOS transistor; and FIGS. **11**, **13**, **15** and **17** illustrate cross-section views of FIGS. **10**, **12**, **14** and **16** along the B-B direction. For illustrated purposes, the exemplary fabrication process shown in FIG. **27** is still used to make the LDMOS transistor.

As shown in FIG. **27**, at the beginning of the fabrication process, a semiconductor substrate with certain structures is provided (S**101**). FIG. **10** illustrates a corresponding semiconductor structure; and FIG. **11** illustrates a cross-section view of the semiconductor structure shown in FIG. **10** along the B-B direction.

As shown in FIG. **10** and FIG. **11**, a semiconductor substrate **301** is provided. The semiconductor substrate **301** may include any appropriate type of semiconductor material, such as single crystal silicon, germanium, poly silicon, amorphous silicon, silicon germanium, carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, alloy semiconductor, or epitaxially grown materials, etc. The semiconductor substrate **301** may also provide a base for subsequent processes and structures.

After providing the semiconductor substrate **301**, a well region **302** may be formed in the semiconductor substrate **301**. The well region **302** may be made of any appropriate material, which may be same as the semiconductor substrate **301**, or different from the semiconductor substrate **301**. If the semiconductor substrate **301** is used to subsequently form N-type LDMOS transistors, the semiconductor substrate **301** may be doped with P-type ions, and the well region **302** may be doped with P-type ions too. If the semiconductor substrate **301** is used to subsequently form P-type LDMOS